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In re U. S. Patent Application)
Serial No.: 09/455991)
Filed: December 6, 1996)
For: SEMICONDUCTOR DEVICE AND)
METHOD OF MANUFACTURING THE SAME)

VERIFICATION OF TRANSLATION

Sir:

I, Etsuko FUJIMOTO, 303 Charm KY, Higashi-Fuchinobe, Sagamihara-shi, Kanagawa-ken 229-0005 Japan, herewith declare:

that I am well acquainted with both the Japanese and English Languages; and that to the best of my knowledge and belief the following is a true and correct translation of the above referenced Japan Patent Application No. 1996-358955 filed on December 30, 1996.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements.

Date: this 18 day of October, 2002

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[Title of Invention] SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

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[List of Attachment]

[Attachment] Specification 1

[Attachment] Drawing 1

[Attachment] Abstract 1

[NAME OF DOCUMENT] Specification

[TITLE OF THE INVENTION] SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

[Claims]

[Claim 1]

A method of manufacturing a semiconductor device, comprising the steps of:

forming an amorphous silicon film on a substrate having an insulating surface;

providing metal element that promote crystallizations of silicon to plural regions on the amorphous silicon film; and

conducting a heat treatment to allow crystal growing in parallel to the substrate from plural metal element added regions;

wherein at least one of the metal element added regions is not used to manufacture devices but used to control crystal growth states grown from another metal element added regions.

[Claim 2]

A method of manufacturing a semiconductor device according to claim 1, wherein the metal elements consist of one or plural kinds of elements selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

[Claim 3]

A method of manufacturing a semiconductor device according to claim 1, wherein the introduction of the metal elements is conducted by an ion implanting method.

[Claim 4]

A method of manufacturing a semiconductor device according to claim 1, wherein the introduction of the metal elements is conducted by coating a solvent in which metal elements are dissolved or dispersed.

[Claim 5]

A semiconductor device disposed on a substrate having an insulating

surface, the semiconductor device comprising:

an active layer formed of a crystalline silicon film where crystal grows in parallel to or substantially in parallel to the substrate from one of a plurality of regions to which metal elements that promote the crystallization of silicon are added;

wherein a crystal growth region where crystal grows from another one of the plurality of regions is not used as an active layer of the semiconductor device.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[TECHNICAL FIELD OF THE INVENTION]

The present invention relates to the semiconductor device using thin crystalline semiconductor film and method of manufacturing the same.

[0002]

[DESCRIPTION OF THE PRIOR ART]

Thin-film transistor (TFT) is a semiconductor device that is manufactured by using the step of depositing a silicon film on a substrate, and used in optical electric devices like an active matrix type liquid crystal display.

[0003]

Especially, because the field emission mobility of polysilicon TFT having a crystalline semiconductor film is higher than the field emission mobility of an amorphous TFT having an amorphous semiconductor film, an active matrix circuit for a liquid-crystal display device and a peripheral drive circuit are formed on a same substrate.

[0004]

There are two types of polysilicon TFT, a high temperature polysilicon TFT and a low temperature polysilicon TFT.

[0005]

A high temperature polysilicon TFT is manufactured using the step of a relatively high temperature annealing process like 800℃, 900℃ or more to make a crystalline silicon film. However, only an expensive quartz substrate that withstands high temperature can be used to manufacture a high temperature polysilicon film.

[0006]

On the other hand, a low temperature TFT can be manufactured using the steps of a thermal annealing process of 600℃ or lower or a laser annealing that hardly causes thermal damage to an inexpensive glass substrate to manufacture a crystalline silicon film.

[0007]

At present, the characteristics of a high temperature polysilicon TFT and a low temperature polysilicon TFT are almost same, the mobility is 50 to 100 (cm^2/Vs) and the S value is 200 to 400 (mV/dec) (V_D = 1V).

[0008]

However, the operation speed of a source driver circuit in a peripheral drive circuit is required to be several tens MHz or more, and the margin of driving speed is only several MHz in case of using a circuit consisting of high temperature TFTs and low temperature TFTs of prior art.

[0009]

Therefore, a method of dividing the operation (which is called divided operation) is used to manufacture liquid crystal display device presently. However, this method has problems like stripe patterns are observed in the screen due to subtle gaps of divided time etc.

[0010]

To solve these problems, the TFT shown in the Japanese Patent Application Laid-Open No. 08-327978 is invented. That is the TFTs using a crystalline silicon film that has crystal structure with

continuity in one direction and grain boundaries along the same direction, and having a superior characteristic like 100 (mV/dec) or less S value and 200 (cm^2/Vs) or more mobility.

[0011]

Then, in case of using these TFTs, a peripheral circuit which can operate high-speed of several tens MHz or more is obtained.

[0012]

[PURPOSE TO BE SOLVED BY THE INVENTION]

Summerizing the art shown in the above-mentioned application,

(1) By conducting a heat treatment after metal elements like nickel are held on some portions on a surface of an amorphous silicon film, crystals are allowed to grow in parallel to the substrate from the metal element added regions.

[0013]

(2) A thermal oxide film is formed by a heat treatment under an atmosphere containing halogen elements therein.

[0014]

(3) The thermal oxide film is removed.

[0015]

(4) Again, a thermal oxide film is formed as a gate insulating film.

[0016]

It is preferable that a direction along which crystal lattices continuously extend is nearly identical with a direction connecting the source region and the drain region.

[0017]

That is because carriers can move easiest in the structure during TFT operation. In other words, in the direction along which crystal lattices continuously extend, crystal continuity is nearly maintained, scattering and trapping of carriers are much less than other directions when the carriers move.

[0018]

As mentioned above, the characteristics of TFTs are determined according to the position between a direction along which crystal lattices continuously extend and a direction of moving carriers, and TFTs with high mobility can be obtained in case these directions are nearly identical.

[0019]

Therefore, it is important to consider the direction connecting the source region and the drain region (a direction of moving carriers during operation) toward the metal elements like nickel added region in case of designing a circuit which is required high-speed operation using above-mentioned TFTs.

[0020]

That is, crystals are allowed to grow in parallel to the substrate from the metal element added region toward a periphery. This direction is a direction along which crystal lattices continuously extend, and it is necessary to arrange TFTs in the manner where this direction and the direction connecting the source region and the drain region are nearly identical.

[0021]

The arrangement pattern shown in Fig. 2 is proposed in case of arranging nickel added regions and TFTs on a substrate as mentioned above.

[0022]

In Fig. 2, TFT 201 to 208 are arranged beside nickel added regions 211 or 212, and each active layers of TFTs are made using the crystalline silicon film (crystal growth regions) grown from each of the nearest nickel added regions. Note that, the directions shown by the arrows 221 to 224 are crystal growth directions.

[0023]

However, a crystal growth distance depends on the interval between the respective nickel added regions, in case the interval is long, the crystal growth distance is short. The difference

of crystal growth distance influences a characteristic of the TFT.

[0024]

A liquid crystal display device has a plurality of same kinds of build-in circuits. To operate several hundreds × several hundreds pixels in a same way, each of these many same kinds of circuits have to operate in a same way. Therefore, the characteristics of the TFTs that consist these circuits must be same.

[0025]

Especially, TFTs 201, 202, 207 and 208 which are formed in the regions not interposed between the nickel added regions may not have enough crystal growth distance or crystallinities. In this case, the mobility of TFTs 201, 202, 207 and 208 become insufficient.

[0026]

That is, comparing TFTs 201 and 203, 203 has characteristic suitable for high-operation speed due to good crystallinity, on the other hand, 201 has characteristic unsuitable for high-operation speed due to not good crystallinity in spite of having same channel type and same size.

[0027]

In case of manufacturing a circuit which is required high-speed operation, enough operation speed may not be obtained due to unbalance of each device characteristics.

[0028]

The purpose to be solved in this specification is correcting the above-mentioned difference of crystal growths and providing same TFT characteristics. Especially, the purpose is providing technique of improving the crystal growth states in the regions not interposed between the nickel added regions.

[0029]

[METHOD TO SOLVE THE PURPOSE]

One of the inventions showing in this specification is comprising the steps of:

forming an amorphous silicon film on a substrate having an insulating surface,

adding metal elements to a plurality of regions selectively; and

conducting a heat treatment to allow crystal to grow in parallel to the substrate from the metal element added regions,

wherein at least one of the metal element added regions is not used to manufacture devices but used to control the state of crystal growth grown from the other regions where metal elements are selectively added.

[0030]

According to above-mentioned structure, the metal elements consist of one or plural kinds of elements selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au can be used.

[0031]

The most preferable one is nickel from the viewpoints of reproducibility and advantages.

[0032]

In the above-mentioned structure, it is preferable that the introduction of the metal elements is conducted by an ion implanting method or coating a solvent in which metal elements are dissolved or dispersed.

[0033]

Another one of the inventions showing in this specification is

a semiconductor device on a substrate having an insulating surface,

an active layer formed of a crystalline silicon film where crystal grows in parallel to or substantially in parallel to the substrate from one of a plurality of regions to which metal elements

that promote the crystallization of silicon are added,

wherein a crystal growth region where crystal grows from another one of the plurality of regions is not used as an active layer of the semiconductor device.

[0034]

[FORM OF THE INVENTION]

One example is that arranging nickel added region 101 to 104 at same intervals, and manufacturing thin-film transistor using the crystalline growth regions grown from regions 102 and 103 as shown in Fig. 1. Note that, arrows 121 to 128 indicate crystal growths.

[0035]

In the way mentioned above, due to the arranging of nickel added regions 101 and 104, the crystal growth distances of crystalline silicon film used as active layers of TFTs 111, 112, 117 and 118 and the crystal growth distances of crystalline silicon film used as active layers of TFTs 113 and 114 become almost same.

[0036]

Note that, nickel added regions 101 and 104 are not arranged in order to crystallize an amorphous silicon film. Theses nickel added regions 101 and 104 are arranged in order to make distances and crystal growth states of 123 and 126 alike to 124 and 125. In other words, they are arranged as dummy regions to control the crystal state of another crystal growth regions, even though they are not used finally.

[0037]

Therefore, the regions which crystal growths are grown from nickel added regions 101 and 104 are not used to manufacture devices.

[0038]

It is important that conducting crystal growths from nickel added regions 101 and 104 gives a preferable influence to another crystal growth regions that are used to manufacture devices

intentionally.

[0039]

In other words, conducting crystal growths from nickel added regions 101 and 104 can control the crystal growth states of crystal growth regions which are used to manufacture semiconductors.

[0040]

In this way, by conducting crystal growths from dummy nickel added regions 101 and 104, it is possible to control the crystal growth distances and crystal states of the crystalline silicon film which is used to manufacture TFTs indicated by reference number 111 to 118.

[0041]

Note that, it is preferable that intervals between the respective nickel added regions are arranged uniform. The reason is that crystal growth distances will change due to the width of nickel added regions, and design parameter will increase.

[0042]

[PREFERRED EMBODIMENTS]

[First Embodiment]

In this embodiment, it is shown that manufacturing process of a TFT using crystalline silicon film which has continuous crystal structure in prescribed direction and grain boundaries aligning toward the prescribed direction, connecting with the position of nickel added regions.

[0043]

Figs. 3 to 5 show the manufacturing process of this embodiment. First, a silicon oxide film 302 is formed in thickness of 3,000 Å on a quartz substrate 301 as an under film. If the surface of the quartz substrate is excellent in smoothness and also satisfactorily cleaned, the under film 302 is not particularly required.

[0044]

Under the existing circumstances, it is a preferable choice to use the quartz substrate as a substrate, however, if it is an insulating substrate that can withstand a heat treatment temperature, the substrate is not limited to quartz.

[0045]

Then, an amorphous silicon film 303 which is a starting film of a crystalline silicon film is formed in thickness of 500 Å through a low pressure CVD method.

[0046]

Thereafter, a silicon oxide film not shown is formed in thickness of 1,500 Å and then patterned to form a mask denoted by reference numeral 304. The mask is opened in regions 305 to 307. In the region where openings 305 to 307 are defined, the amorphous silicon film 303 is exposed.

[0047]

Note that, the opening 307 is a dummy region of Nickel added region.

[0048]

The openings 305 to 307 are shaped in a slender rectangle which is longitudinal backward and frontward of the drawing. It is proper that widths of the openings 305 to 307 are set to 20 μm or more. Also, the lengths can be determined as needed.

[0049]

Nickel acetate solution containing nickel elements of 10 ppm in weight conversion therein is coated on the surface. Then, spin dry is conducted using a spinner not shown to remove a surplus solution. The amount of introduced nickel element can be controlled by the nickel element concentration of above-mentioned solution.

[0050]

In the above manner, a state in which the nickel elements exist in a state indicated by a dotted line 308 of Fig. 3(A) is

obtained. In this state, the nickel elements are held selectively in contact with a part of the amorphous silicon film on bottoms of the openings 305 to 307.

[0051]

The introduction of nickel elements may be conducted through the ion implanting method. In this case, a position at which the nickel elements are introduced can be controlled with higher accuracy in comparison with a case in which a nickel element solution is coated on the surface. Therefore, this is effective particularly in a case where a width of a region into which the nickel elements are introduced is extremely narrow to the degree of several μm or less, or in a case where a shape of the introduced region is complicated.

[0052]

Subsequently, a heat treatment is conducted at 500 to 630 ℃, for example, 600 ℃ for 8 hours in a nitrogen atmosphere containing hydrogen of 3% but little of oxygen. With this process, crystal growth is progressed in parallel to the substrate 301 as indicated by reference numeral 309 in Fig. 3(A).

[0053]

The crystal growths are progressed from regions of the openings 305 to 307 into which the nickel elements are introduced toward a periphery thereof. This crystal growth, which is parallel to the substrate, is called lateral growth.

[0054]

Then, the mask 304 which is formed of the silicon oxide film for selectively introducing the nickel elements is removed.

[0055]

In this state, the nickel elements are segregated in the crystalline silicon film. In particular, the nickel elements exist with a relatively high concentration in the regions where the openings

305 to 307 are defined and a top portion of the crystal.

[0056]

Therefore, in formation of the active layer, it is important to prevent those regions. That is, it is important to prevent the regions in which the nickel elements are segregated from existing in the active layer.

[0057]

After the crystallization, a laser beam may be applied to the surface. In other words, crystallization may be further promoted by the application of a laser beam. The application of the laser beam has an effect of diffusing a lump of nickel elements that exist in the film so as to be liable to remove the nickel elements later. Even if a laser beam is applied at this stage, the lateral growth is not further progressed.

[0058]

The laser beam can be obtained by using an eximer laser having a wavelength of an ultraviolet region. For example, an KrF eximer laser (248 nm in wavelength) or an XeCl eximer laser (308 nm in wavelength) can be used.

[0059]

Thereafter, a heat treatment is conducted at 950 ℃ under an oxygen atmosphere containing halogen elements therein, for example, an oxygen atmosphere containing HCl of 3 volume % to form a thermal oxide film not shown having a thickness of 200 Å. With the formation of the thermal oxide film, the thickness of silicon film is reduced about 100 Å. In other words, the thickness of the silicon film becomes about 400 Å.

[0060]

In general, while thermal oxide is formed on the silicon surface, increased thickness toward surface is appropriate same as the

distance gone toward inside. Therefore, in case 100Å thermal oxide is formed on the surface of 100Å silicon, the thickness of silicon decrease 50 Å to become 50 Å silicon film and 100 Å thermal oxide is formed on the surface.

[0061]

In the above process, during the formation of the thermal oxide film, the silicon elements having an unstable bonding state in the film is used to form a thermal oxide film. Then, defects in the film are reduced and higher crystallinity is obtained.

[0062]

At the same time, during the formation of the thermal oxide film, the gettering of the nickel elements from the film is conducted due to the effect of chlorine.

[0063]

It is needless to say that the nickel elements are taken in the thermal oxide film with a relatively high concentration. Then, the nickel elements in the silicon film are relatively reduced.

[0064]

And then, the thermal oxide film is removed. As a result, a crystalline silicon film having the reduced concentration of the nickel elements contained therein is obtained.

[0065]

The crystalline silicon film thus obtained has a structure in which a crystal structure extends in one direction (this direction is identical with an orientation of crystal growth). In other words, a plurality of slender cylindrical crystals are structured to be aligned in parallel through a plurality of grain boundaries that extend in one direction.

[0066]

Then, patterning is conducted to form a pattern 310 which is formed by a lateral growth region. The island region 310 will

be formed into an active layer of the TFT later.

[0067]

In this process, a pattern is positioned in a condition that a direction connecting the source region and the drain region is identical with or nearly identical with an orientation of crystal growth. With this process, the direction of moving carriers can be identical with the direction along which crystal lattices continuously extend, as a result, a TFT with high characteristic can be obtained.

[0068]

Then, after the formation of the pattern 310, a thermal oxide film 311 is formed in thickness of 300 Å. This thermal oxide film is obtained by conducting a heat treatment of 950 ℃ in an oxygen atmosphere containing HCl of 0.1 to 10 volume%, for example, 3% therein.

[0069]

With the formation of the thermal oxide film 311, the thickness of the pattern (a pattern which is formed into an active layer) 310 becomes 250 Å.

[0070]

In this process, the same effect as forming the thermal oxide film, which was removed, can be obtained. The thermal oxide film 311 is formed into a part of the gate insulating film of the TFT.

[0071]

In this embodiment, the final obtained thickness of active layer 310 consisting of crystalline silicon (250 Å) is thinner than the thickness of second thermal oxide film 311 (300 Å). Due to this structure, the effect to get crystalline structure having continuity in prescribed direction and crystalline grain boundaries grown in the direction is obtained.

[0072]

Thereafter, a silicon oxide film 312 which form the gate insulating film with the thermal oxide film is formed in thickness of 1,000 Å through the plasma CVD method (Fig. 3(B)).

[0073]

The concentration of nickel that finally remains in a silicon film is about 1×10^{14} atom/cm^3 to 5×10^{18} atom/cm^3 in the existing circumstances, but more preferable as it is low. Researching the best conditions of gettering during the formation of a thermal oxide film, the upper limit of the concentration can be reduced up to about 5×10^{17} atom/cm^3. The measurement of the concentration can be performed employing an SIMS (secondary ion mass spectroscopy).

[0074]

Then, an aluminum film for forming a gate electrode is formed in thickness of 4,000 Å through the sputtering method. Scandium of 0.2 weight% is contained in the aluminum film.

[0075]

The reason why scandium is contained in the aluminum film is to suppress the occurrence of hillock or whisker during a post-process. The hillock and whisker are directed to a needle-shaped or shaped projection which is caused by abnormal growth of aluminum during heating.

[0076]

A material used for forming the gate electrode other than aluminum may be tantalum (Ta), polycrystal silicon which is doped with a large amount of phosphorus (P), silicide of tungsten (WSi), or a lamination layer or mixture of polycrystal silicon which is doped with phosphorus and silicide of tungsten.

[0077]

After the formation of the aluminum film, a fine anodic oxide film not shown is formed. The anodic oxide film is formed in an

ethylene glycol solution containing tartaric acid of 3% therein as an electrolyte with aluminum as an anode and platinum as a cathode. In this process, the anodic oxide film having a fine quality is formed in thickness of 100 Å on the aluminum film.

[0078]

The fine anodic oxide film not shown serves to improve an adhesion to a resist mask which will be formed later.

[0079]

The thickness of the anodic oxide film can be controlled according to supply voltage during anodic oxidation.

[0080]

Subsequently, a resist mask 313 is formed. Then, using the resist mask 313, the aluminum film is patterned into a pattern indicated by 314. Thus, a state shown in Fig. 4(C) is obtained.

[0081]

In this stage, anodic oxidation is again conducted. In this situation, oxalic acid aqueous solution of 3% is used as an electrolyte. In the electrolyte, anodic oxidation is conducted with the aluminum pattern 314 as an anode, to thereby form a porous anodic oxide film 315.

[0082]

In this process, the anodic oxide film 315 is selectively formed on the side surfaces of the aluminum pattern because the high-adhesive resist mask 306 exists on the upper side.

[0083]

The anodic oxide film can be allowed to grow up to several μm in thickness. In this example, the thickness of the anodic oxide film is set to 6,000 Å. The growth distance can be controlled according to an anodic oxidizing time.

[0084]

Then, the resist mask 314 is removed. Thereafter, a fine

anodic oxide film is again formed. In other words, anodic oxidation is again conducted in the above-mentioned ethylene glycol solution containing tartaric acid of 3% therein.

[0085]

In this process, an anodic oxide film 316 having a fine quality is formed because the electrolyte enters the porous anodic oxide film 315 as shown in Fig 4(D).

[0086]

The thickness of the fine anodic oxide film 316 is set to 1,000 Å. The thickness of the anodic oxide film can be controlled according to supply voltage.

[0087]

In this situation, the exposed silicon oxide film 312 is etched. At the same time, the thermal oxide film 311 is etched. The etching as used is a dry etching. Then, using a mixed acid where acetic acid, nitric acid and phosphoric acid are mixed together, the porous anodic oxide film 315 is removed. Thus, a state shown in Fig. 5(E) is obtained.

[0088]

After the state shown in Fig. 5(E) is obtained, impurity ions are implanted. In this process, in order to fabricate an n-channel type thin-film transistor, P (phosphorus) ions are implanted through the plasma doping method.

[0089]

In this process, region 319 which is a heavy-doped region and 320 which is a light-doped region are formed. This is because the remaining silicon oxide film 318 functions as a semi-transparent mask, and a part of the implanted ions is shielded by the film.

[0090]

Then, a laser beam (or an intense light by a lamp) is applied to activate the region into which the impurity ions are implanted. Thus, a source-drain region 319, a channel formation region 321,

and low concentration impurity region 320 are formed in a self-aligning manner (Fig 5(E)).

[0091]

In the case where the thickness of the fine anodic oxide film 316 is thickened to 2,000 Å or more, offset gate regions can be formed by this thickness outside of the channel formation region 321.

[0092]

Similarly, in this embodiment, the offset gate region is formed. However, since its dimensions are small such that a contribution of the offset gate region is small, and also the drawings are complicated, the offset gate region is omitted from the drawing.

[0093]

In order to make the anodic oxide film having the fine quality thicker to the degree of 2,000 Å or more, since a supply voltage of 200 V or higher is required, attention must be paid to reproducibility and safety.

[0094]

Subsequently, a silicon oxide film, a silicon nitride film or a lamination film consisting of those films is formed as an interlayer insulating film 322. The interlayer insulating film may consist of a layer which is made of a resin material on a silicon oxide film or a silicon nitride film.

[0095]

Then, contact holes are formed so that a source electrode and a drain electrode 323 are formed. Thus, a thin-film transistor shown in Fig. 5(F) is completed.

[0096]

The TFT according to this embodiment has an extremely high characteristic which could not be obtained by the conventional TFT.

[0097]

For example, an NTFT (n-channel type TFT) as manufactured has a high performance such as the mobility of 200 to 300 (cm^2/Vs) and the S value of 75 to 90 (mV/dec) (V_D = 1 V). A PTFT (p-channel type TFT) as manufactured has a high performance such as the mobility of 120 to 180 (cm^2/Vs) and the S value of 75 to 100 (mV/dec) (V_D = 1 V).

[0098]

In particular, the S value is a wonder excellent value which is 1/2 or less of that in the conventional high-temperature polysilicon TFT and low-temperature polysilicon TFT.

[0099]

The TFT thus manufactured can conduct the operation of 1 GHz in a ring oscillator level and the operation of 100 MHz in the shift register level when a voltage of the drive signal is 3.3 to 5 V.

[0100]

Also, because of the existence of dummy nickel added region 307, the crystal growth distance becomes sufficiently long and TFT with above-mentioned characteristic is obtained.

[0101]

Further, in case the intervals between the respective nickel added regions are unified, the characteristics of the TFTs 501 to 503 are also substantially identical with each other.

[0102]

Also, the thin-film transistor employing the crystalline silicon film having the above singular crystal structure is characterized in that the crystal structure makes it hard to exhibit the short channel effect. Also, it is characterized in that since an insulator is used as a substrate, there rises no problem on the capacity of the substrate, and it is suitable for high-speed

operation.

[0103]

The conventional MOS transistor using a monocrystal silicon wafer has a scaling rule. This is that as the dimensions of the transistor are made small in accordance with a predetermined rule, the performance of the transistor is enhanced in accordance with the predetermined rule.

[0104]

However, under the circumstances where the fining of the transistors has been greatly advanced in recent years, it becomes difficult to enhance the performance of the transistor in accordance with that scaling rule.

[0105]

As one example, as a channel length is shortened to suppress the short channel effect, a fine measure such that a portion along the channel is doped with impurities is required, thereby more increasing the difficulty in a manufacture process.

[0106]

However, in the case of using a crystalline silicon film having such a singular crystal structure, a required characteristic can be obtained by the dimensions which are not complied with the above scaling rule.

[0107]

It is presumed that this is caused by items stated below.

(1) A direction along which a columnar crystal extends is identical with a direction of moving carriers in the channel, to thereby suppress the short channel effect.

(2) An insulator is employed for a substrate, to thereby greatly suppress a problem on the capacity.

(3) Since the gate electrode can be made of aluminum, it is advantageous in the high-speed operation.

[0108]

In the item (1), the following can be presumed. That is, each columnar crystal structure is partitioned by an inactive grain boundary. Since the grain boundary portion is high in energy level, the movement of the carriers is regulated along the crystal extending direction. Also, in the same way, the spread of a depletion layer into the interior of the channel from the source and drain regions is suppressed. It is presumed that this suppresses the short channel effect.

[0109]

Specific examples in which the characteristics are not complied with the above-mentioned scaling rule are stated below.

[0110]

For example, in the case where the thickness of the gate insulating film must be 100 Å in accordance with the conventional scaling rule, if a crystalline silicon film according to the present invention is used, the same characteristics can be obtained with the thickness of the gate insulating film being 300 Å. As a result, the static electricity resistant characteristic can be enhanced.

[0111]

It is understood that this is caused by the above items (1) to (3).

[0112]

Also, not only the thickness of the gate insulating film but also the channel length can provide a predetermined characteristic under the condition more lenient than the conventional scaling rule (condition lower one rank).

[0113]

This is useful in the case where the semiconductor circuit that enables high-speed operation is manufactured over large area

at the low costs.

[0114]

[Second Embodiment]

What is shown in Fig. 6 is a diagram showing a part of a buffer circuit section within a source driver circuit in a liquid-crystal display device. In particular, this figure shows an end portion of the entire buffer circuit section, in which two invertor circuits 601 and 602 are disposed on an endmost portion, and the same circuits and nickel added regions are cyclically arranged on a lower side of the figure. An equivalent circuit diagram of Fig. 6 is shown in Fig. 7.

[0115]

In Fig. 6, reference numeral 611, 612 and 613 denote nickel added regions. Also, reference numeral 621 denotes a pattern of a crystalline silicon film, 622 is a gate line, 623, 624 and 625 are source or drain lines.

[0116]

The characteristics of the TFT that constitutes invertor circuits (for example, 603, 604 and so on) fabricated under the nickel added region 612 are sufficient. This is because since they are disposed between the respective nickel added regions, a distance of crystal growth of the silicon film in the region therebetween is sufficient.

[0117]

Also, since intervals between the respective nickel added regions are unified, the characteristics of the TFTs are also substantially identical with each other.

[0118]

On the other hand, the invertor circuits 601 and 602 are circuits disposed on the endmost portion, and in order to obtain a sufficient characteristic of the TFTs that constitute those circuits, a dummy nickel added region 611 is disposed as shown in Fig. 6.

[0119]

In particular, an object of this embodiment is to obtain a sufficient characteristic of the TFT that constitutes the invertor circuit 601 which is disposed on the endmost portion. This is because in the case where crystal growth is insufficient, the characteristic of the above TFT is most deteriorated.

[0120]

In this example, the respective intervals between the nickel added regions 611, 612 and 613 are made identical with each other.

[0121]

Since the dummy nickel added region 611 is disposed as mentioned above, the distance of crystal growth of the silicon film in the regions where the TFTs that constitute the invertor circuits 601 and 602 are disposed is made sufficiently long, thereby being capable of obtaining a sufficient characteristic of the TFTs.

[0122]

Then, the operating speed of the invertor circuits 601 and 602 which are disposed on the endmost portion can be sufficiently increased.

[0123]

Furthermore, the characteristic of the TFTs that constitute the invertor circuits 601 and 602 is made identical with the characteristic of the TFT that constitutes the invertor circuit fabricated under the nickel added region 602, thereby being capable of obtaining a plurality of buffer circuits having substantially the same operating speed.

[0124]

[Third Embodiment]

In this embodiment, the structure described in the first and second embodiments is made up of inverted stagger type thin-film transistors. Even if the planner type thin-film transistor in the respective embodiments is replaced by the inverted stagger type thin-film transistor, the same effect can be obtained.

[0125]

As the gate electrode of the inverted stagger type thin-film transistor, to use a material high in heat resistance, for example, polycrystal silicon which is doped with a large amount of phosphorus for the gate electrode is effective in obtaining a high-performance thin-film transistor.

[0126]

[Effect of this invention]

According to the present invention, there can be provided a TFT which corrects a difference in crystal growth due to a distance between the nickel added regions and is uniform in characteristic

using the crystalline silicon film which is fabricated by utilizing nickel addition. In particular, a distance of crystal growth in the region which is not interposed between the nickel added regions can be made sufficiently long.

[0127]

Then, in the liquid-crystal display device, the operating characteristics of the circuits of the same type can be identified so that a large number of pixels can be operated in the same manner.

[0128]

The present invention not only constitutes the peripheral circuit formed on the same substrate as the active matrix circuit in the transmission type or reflection type active matrix liquid-crystal display device, but also is applicable to a display unit employing an EL (electro luminescence) element and a variety of circuits using the thin-film transistors.

[BRIEF DESCRIPTION OF FIGURES]

[Fig. 1] a diagram showing an arrangement of nickel added regions and TFTs of this invention;

[Fig. 2] a diagram showing an arrangement of nickel added regions and TFTs of prior art;

[Figs. 3] diagrams showing a manufacturing process of thin-film transistors;

[Figs. 4] diagrams showing a manufacturing process of thin-film transistors;

[Figs. 5] diagrams showing a manufacturing process of thin-film transistors;

[Fig. 6] a diagram showing an arrangement of nickel added regions and TFTs in buffer circuit;

[Fig. 7] a diagram showing the equivalent circuit of Fig. 6.

[DESCRIPTION OF MARKS]

101 to 104 nickel added regions

111 to 118 TFTs

121 to 128 crystalline growth directions

301 quartz substrate

302 under film (silicon oxide film)

303 amorphous silicon film

304 mask formed of the silicon oxide film

305, 306 nickel added regions

307 dummy nickel added region

308 nickel element

309 crystalline growth direction

310 pattern of crystalline silicon film consisting of active layer

311 thermal oxide film

312 silicon oxide film

313 resist mask

314 pattern consisting of aluminum film

315 porous anodic oxide film

316 fine quality anodic oxide film

317 gate electrode

318 silicon oxide film remained

319 source region, drain region

320 light-doped region

321 channel formed region

322 interlayer insulating film

323 source electrode, drain electrode

[NAME OF DOCUMENT] Document of abstract

[ABSTRACT]

[PURPOSE]

The purpose is to provide same characteristic TFTs using the crystalline silicon film that is fabricated by utilizing nickel addition wherein differences in crystal growth are corrected. In particular, a distance of crystal growth in the region which is not interposed between the nickel added regions can be made sufficiently long.

[METHOD TO ATTAIN THE PURPOSE]

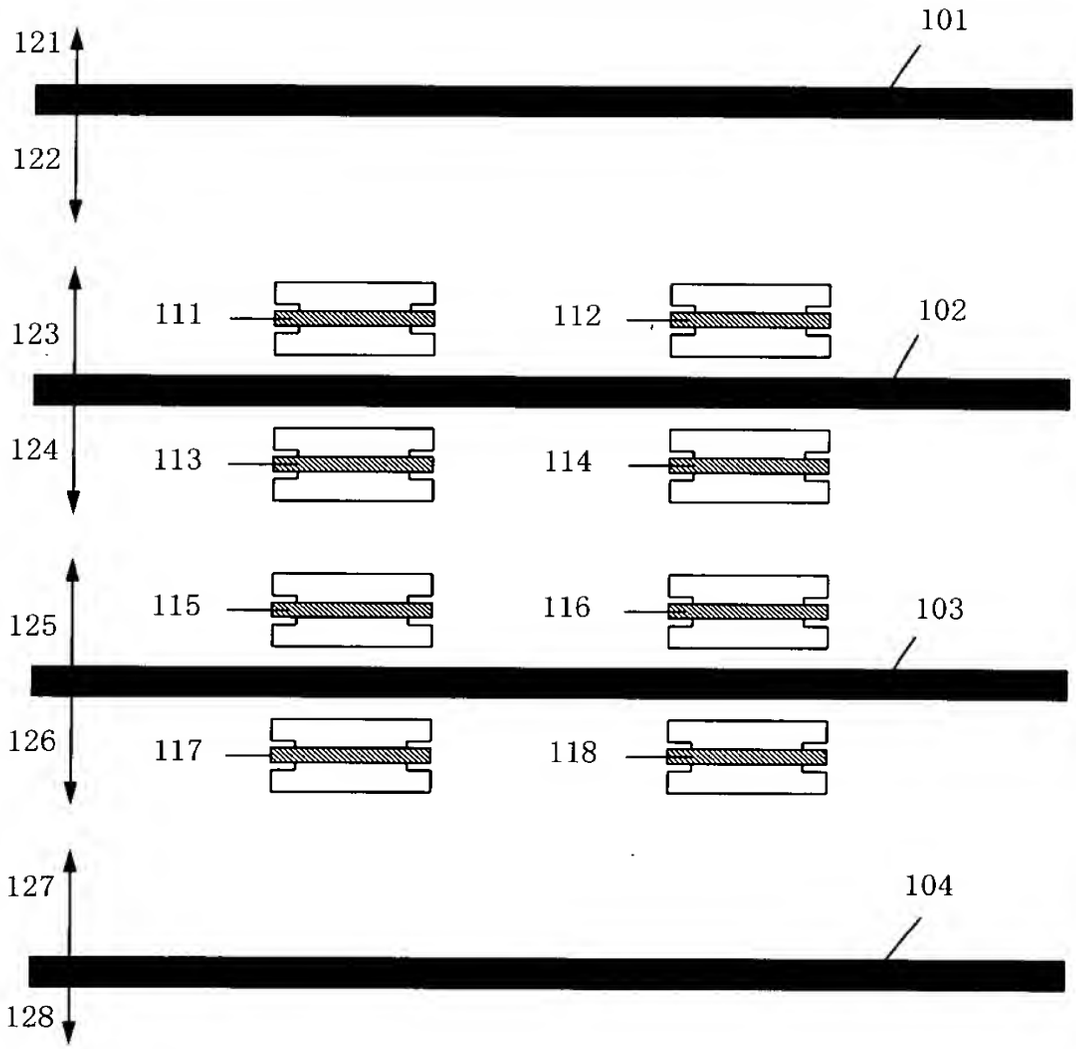
As for the region which is not interposed between the nickel added regions, another nickel added region is formed (as a result, the region become interposed between the nickel added regions). Further, it is preferable that all the intervals between the respective nickel added regions are unified.

[SELECTED FIGURE] Fig. 1

【Refernce Number】 P00352-05

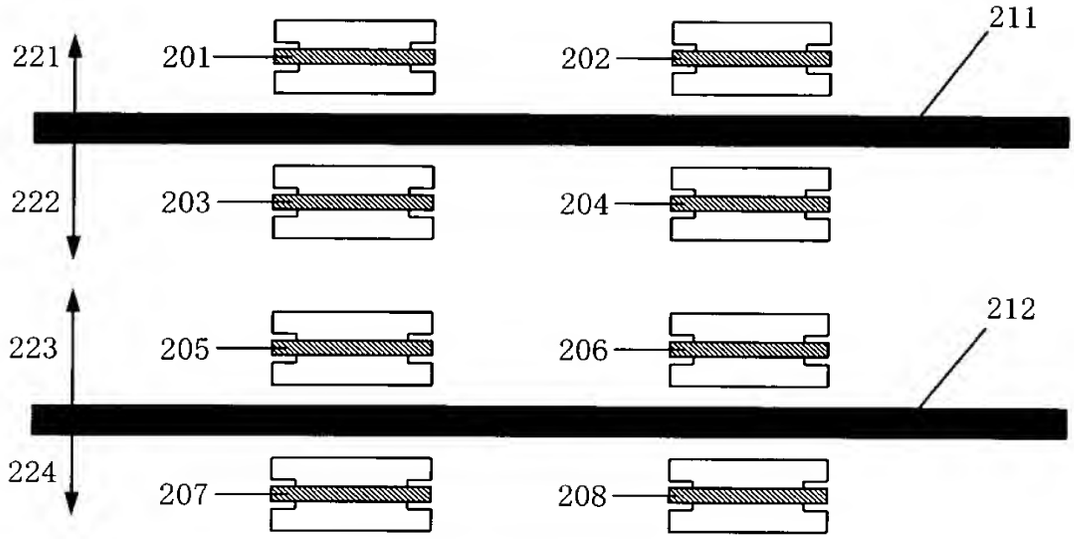
【Document】 Figures

【Fig. 1】



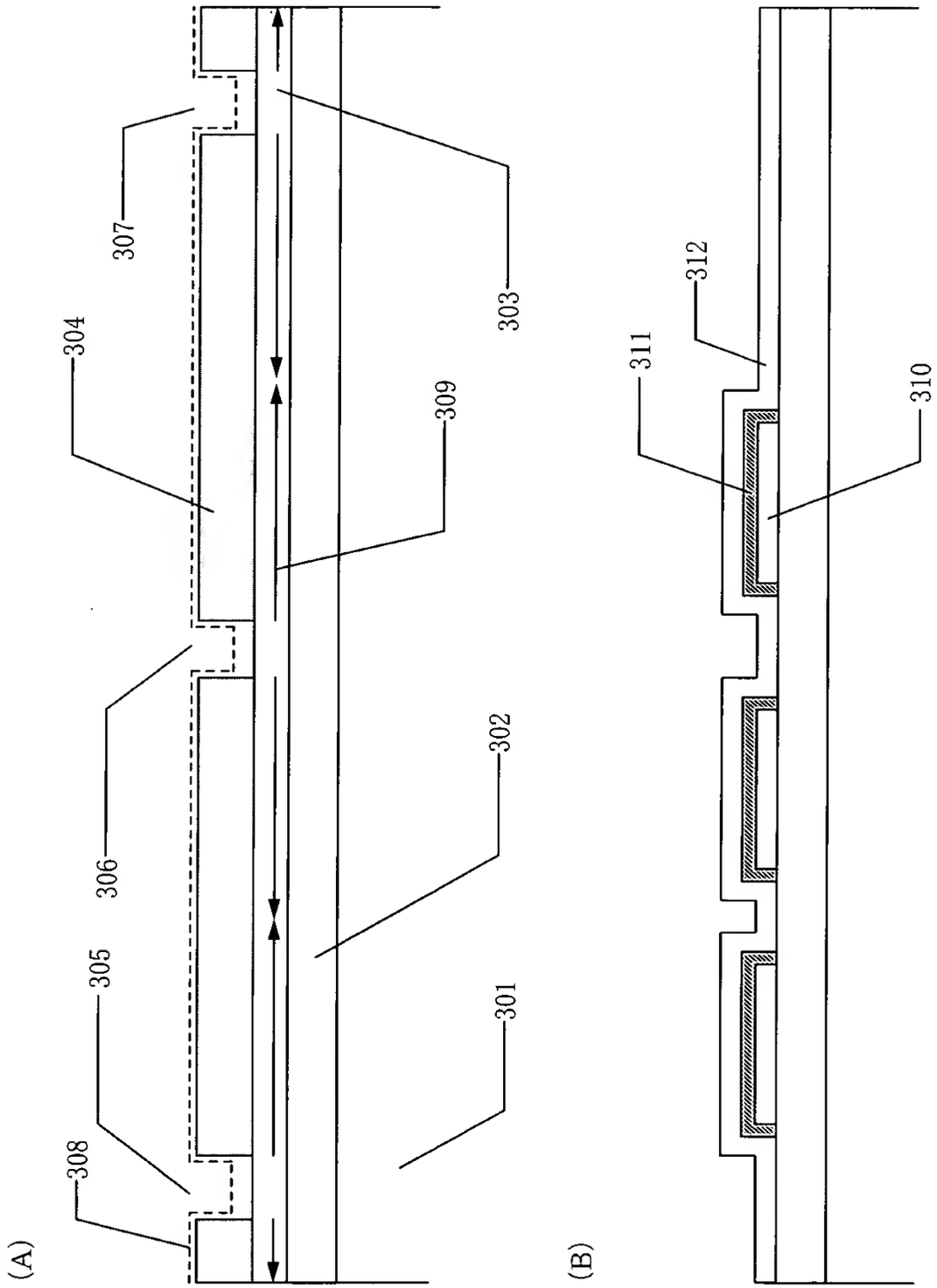
【Reference Number】 P003522-05

【Fig. 2】

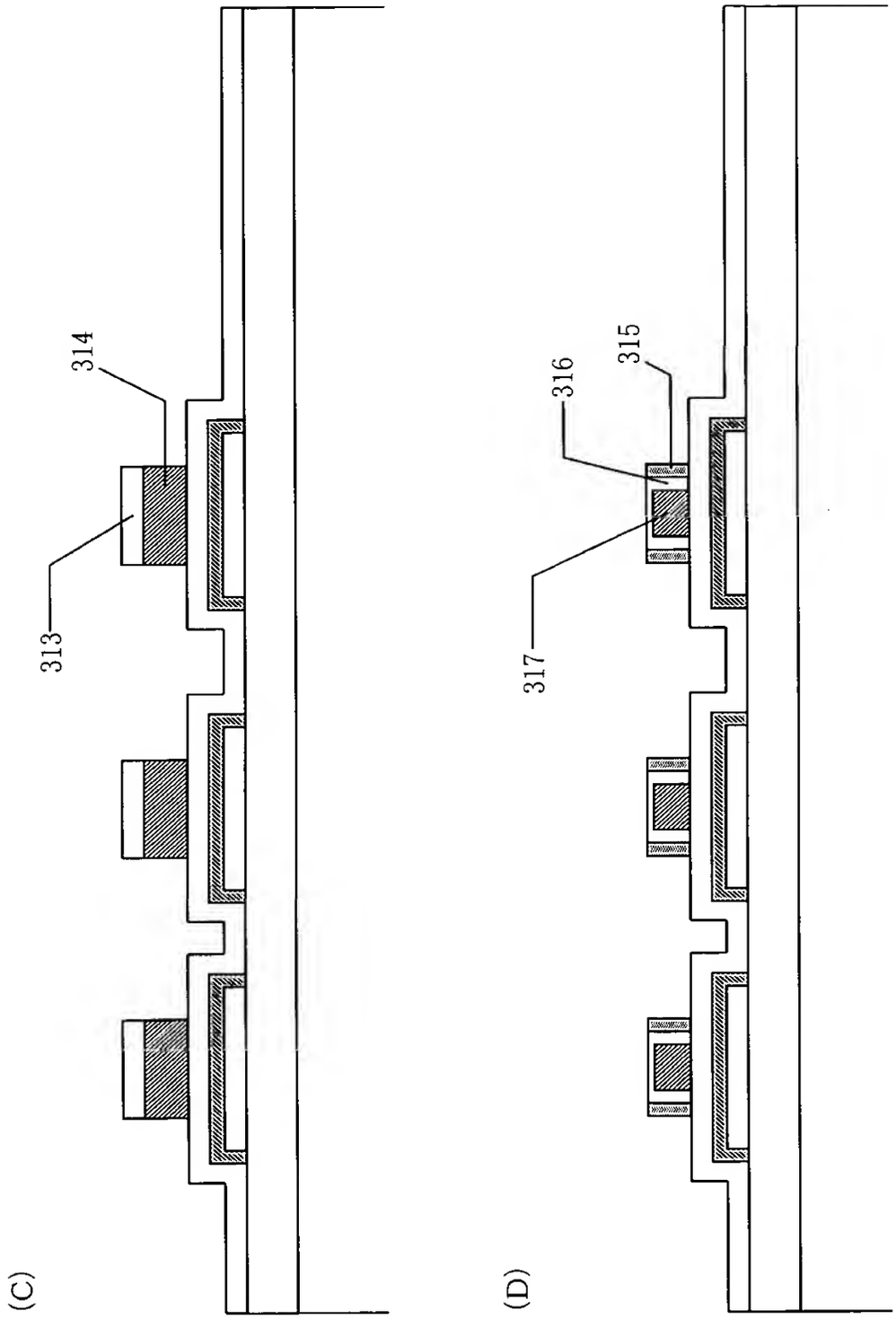


【Referecne Number】 P003522-05

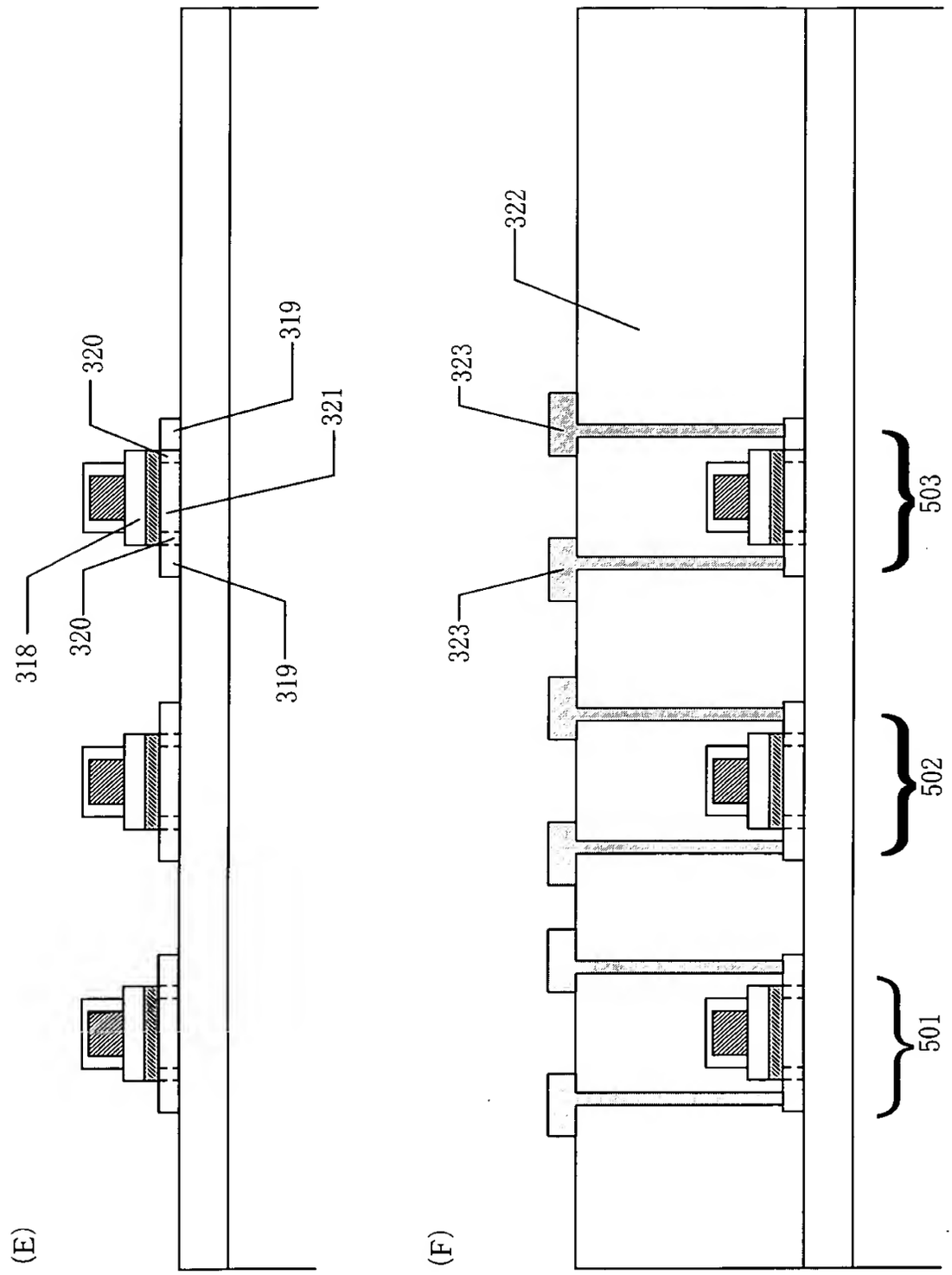
【Figs. 3】



【Figs. 4】

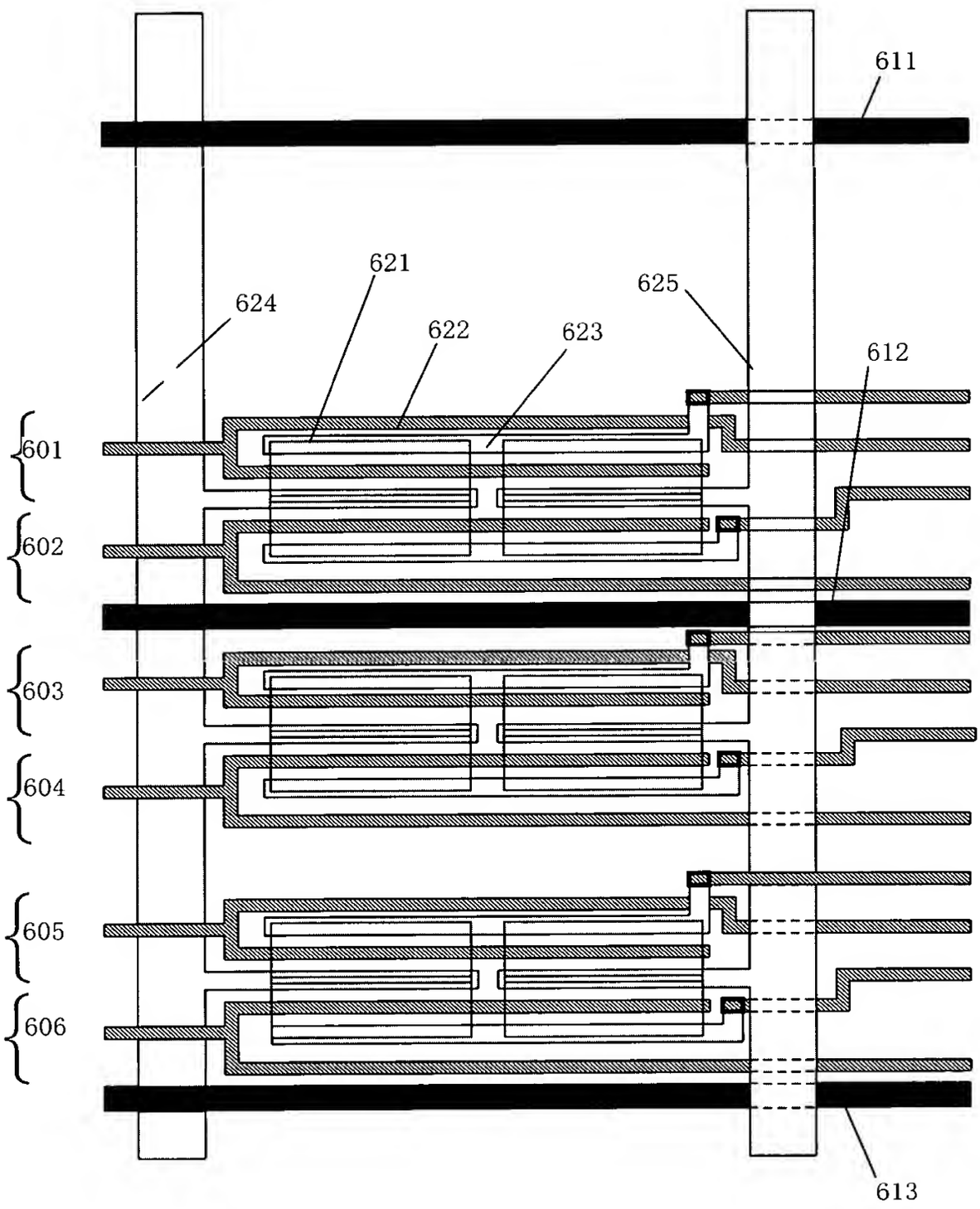


【Figs. 5】



【Reference Number】 P003522-05

【Fig. 6】



【Reference Number】 P003522-05

【Fig. 7】